10/661,745

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NOV 26 2004
PATENT & TRADEMARK OFFICE

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application:
Application No.:
Filed:
Title:
Commissioner for patents
Washington, D.C. 20231

POWER OF ATTORNEY BY ASSIGNEE OF ENTIRE INTEREST
(REVOCATION OF PRIOR POWERS)

As assignee of record of each of the patent applications listed in the table of attachment A,

REVOCATION OF PRIOR POWERS OF ATTORNEY

all powers of attorney previously given in each of the listed patent applications are hereby revoked, and

NEW POWER OF ATTORNEY

the following attorneys/agents are hereby appointed to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith: I hereby appoint all attorneys of Thomas, Kayden, Horstemeyer & Risley, LLP, who are listed under the USPTO Customer Number shown below as the attorneys to prosecute this application and to transact all business in the United States Patent and Trademark Office connected therewith, recognizing that the specific attorneys listed under that Customer Number may be changed from time to time at the sole discretion of Thomas, Kayden, Horstemeyer & Risley, LLP, and request that all correspondence about the application be addressed to the address filed under the same USPTO Customer Number.

000047390
Patent Trademark Office

Please direct all future correspondence and telephone calls to:

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ASSIGNEE OF ENTIRE INTEREST
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Hsinchu, Taiwan 300-77, R.O.C.

ASSIGNEE CERTIFICATION

The certification under 37 C.F.R. §3.73(b) establishing the right of assignee to take action is attached hereto along with documentation evidencing same. Further, in my official position with Taiwan Semiconductor Manufacturing Company, Ltd., I am authorized to sign documents and otherwise act on its behalf in connection with the management and handling of patent applications and other intellectual property matters.

Date: October 14, 2004

Chien-Wei (Chris) Chou
Director - Intellectual Property Division

Attachment A

No.	Serial No	TSMC No.	Application Title	Filing Date	Assignment (Reel/Frame)
1.	10/757,203	2003-0265	Novel Random Access Memory (RAM) Capacitor In Shallow Trench Isolation With Improved Electrical Isolation To Overlying Gate Electrodes	1/14/2004	014898/0605
2.	10/444,874	2002-0161	Silicon Strain Engineering Accomplished Via Use Of Specific Shallow Trench Isolation Fill Materials	5/23/2003	014114/0945
3.	10/358,632	2001-1239	Integration Method To Enhance P+ Gate Activation	2/5/2003	013744/0214
4.	10/224,186	2000-0525	Defocus-Invariant Exposure For Regular Patterns	8/20/2002	014166/0341
5.	10/207,545	2001-0623	Novel Method For Four Direction Low Capacitance ESD Protection	7/29/2002	013145/0728
6.	10/125,215	2001-0475	Printable Assist Lines And The Removal Of Such	4/18/2002	012835/0800
7.	10/150,834	2001-0752	Support For Protecting Containers Holding Breakable Substrates	5/17/2002	012923/0843
8.	10/286,231	1999-0038	Radiation Correction Method For Electron Beam Lithography	11/1/2002	013464/0449
9.	10/290,622	2002-0229	Design Concept For SRAM Read Margin	11/8/2002	013486/0593
10.	10/661,745	2001-1507	Trapezoid Floating Gate To Improve Program And Erase Speed For Split Gate Flash	9/12/2003	014500/0756
11.	10/313,500	2002-0122	Method Of Forming A Novel Composite Insulator Spacer	12/6/2002	013562/0139
12.	10/267,269	1999-0235	Poly Gate Silicide Inspection By Back End Etching And By Enhanced Gas Etching	10/9/2002	Recorded 010229/0291 at the parent application USP 6482748
13.	09/550,260	1999-0509	Quick Method To Examine Oxide Residue At Substrate Contact Hole By High Temperature KOH Dip	4/17/2000	010758/0334
14.	09/695,659	2000-0161	Equipment Forecast System	10/25/2000	011291/0516

Date: October 14, 2004

Chien-Wei (Chris) Chou
Director - Intellectual Property Division